

# Filament-free Multilayer Bulk RRAM for Energy Efficient Compute in Memory

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Filamentary resistive switching mechanisms in conventional RRAM technologies introduce variability, noise, and endurance limitations that hinder their deployment in neuromorphic and compute in memory systems. We present a filament-free bulk-switching RRAM (b-RRAM) technology that overcomes these challenges through systematic engineering of a trilayer metal-oxide stack [1,2]. By tuning the oxygen vacancy distribution across a  $\text{TiO}_x$  switching layer and integrating an AI-Ti-O tunnel barrier, we achieve stable filament-free resistive switching with strong nonlinearity, high retention and endurance without use of a compliance current.

Device-level characterization demonstrates multi-level resistance states up to 128 levels at  $\text{M}\Omega$ -regime, enabled by the bulk switching mechanism. A compact physics-based model is developed, accurately capturing both DC and pulsed switching behaviors and enabling reliable circuit- and system-level simulations [3].

We integrate b-RRAM crossbars into a neuromorphic compute-in-memory platform to implement two edge-AI workloads: (1) a spiking neural network for real-time autonomous navigation, and (2) a dendritic computation-based few-shot learning algorithm leveraging behavioral time-scale plasticity. The platform supports on-chip, continual weight updates and rapid learning from few samples.

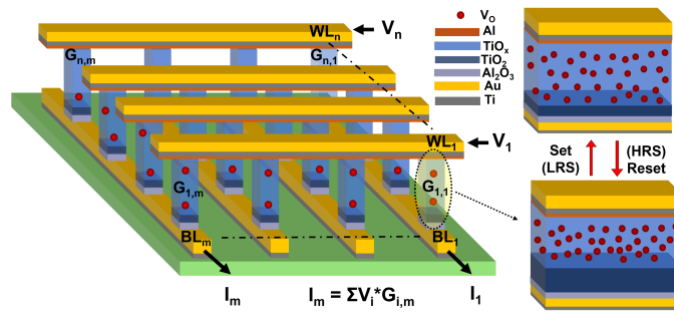
This work demonstrates the potential of filament-free b-RRAM for reliable, energy-efficient compute in memory and neuromorphic computing applications under tight area and power constraints, addressing key scalability barriers of filamentary RRAM.

## References

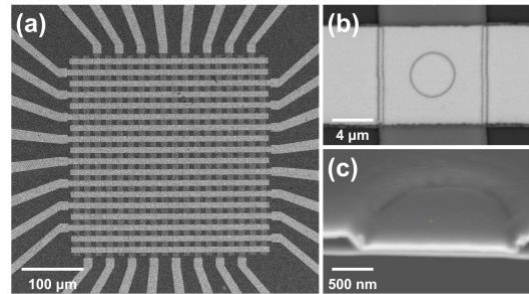
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**Fig. 1.** Schematic of a trilayer b-RRAM crossbar array illustrating MVM operations. Schematics on the right explain Set & Reset switching in b-RRAM stack through modulation of oxygen vacancy ( $V_O$ ) distribution.



**Fig. 2.** SEM images of fabricated (a) 16×16 crossbar array (b) Single b-RRAM device, (c) Cross-section of half-cut b-RRAM device.